ATLAS Liquid Argon Calorimeter Upgrades for HL-LHC

Development of Readout Electronics

Laura Gonzalez Escudero
Supervisor: Brigitte Vachon
McGill University

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ATLAS in the High Luminosity (HL) LHC

Physics Prospects

- Extend **sensitivity** of searches for beyond-the-Standard-Model processes
- Improve precision of **Higgs boson** measurements
  - Higgs boson self-coupling

- The LHC is due to undergo a major upgrade 2026-2029
  - Increase **luminosity** up to a factor of ~5-7
  - Increase p-p **collisions** to ~200 per beam crossing

Technical Challenges

- Address aging of detector and radiation tolerance
- New HL-LHC trigger system

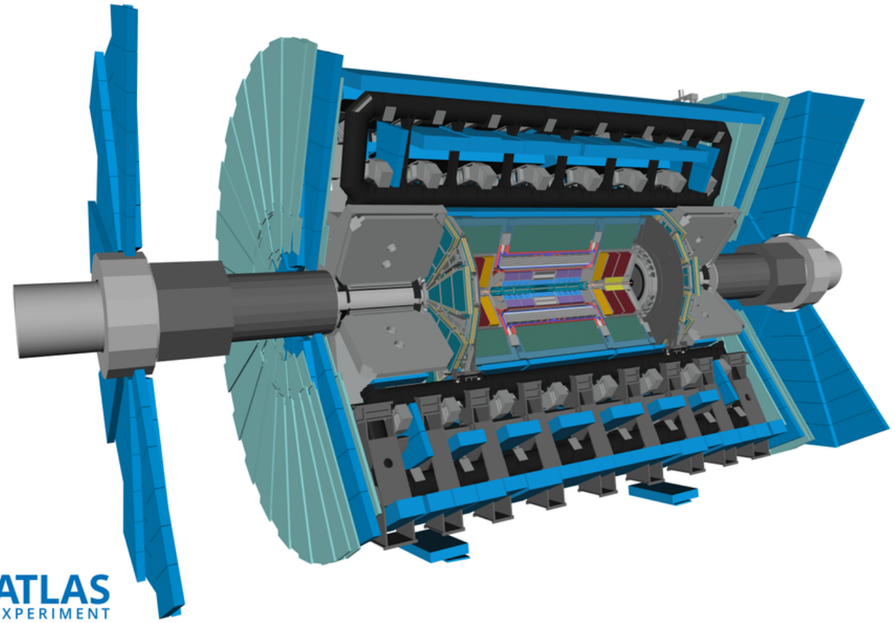
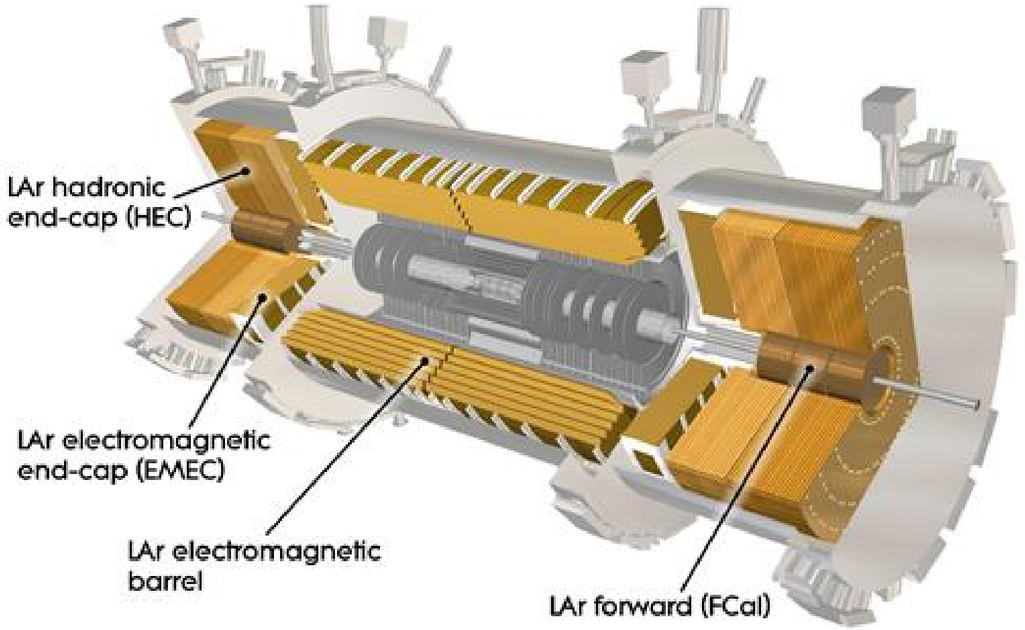


Figure: ATLAS detector. ATLAS-PHOTO-2022-055-2

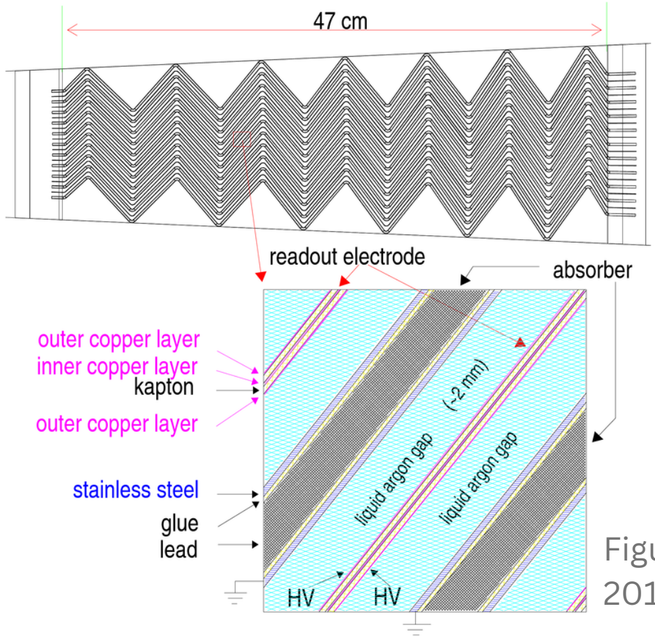
The **L**iquid **Ar**gon Calorimeter within ATLAS

- Sampling calorimeter
  - Energy of electromagnetic showers
- Liquid argon as active material with metal layers



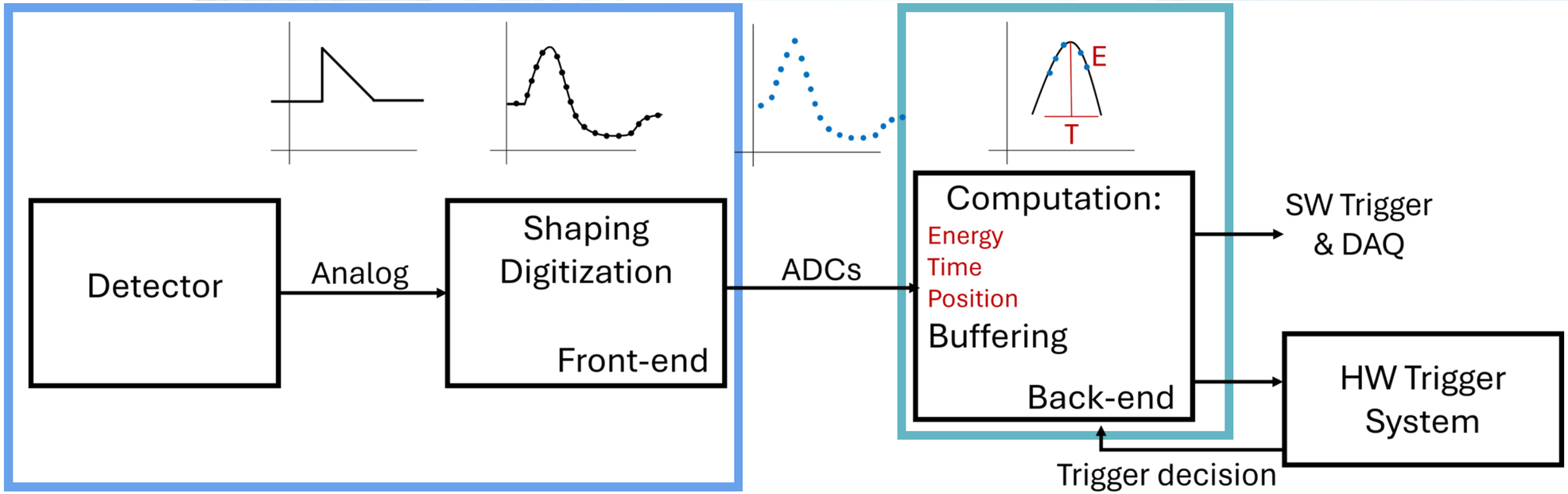
Technical Challenges

- Increased **radiation dose**
- New **trigger and data acquisition** schemes needed
  - Faster trigger rates
  - Longer buffer times
  - Send refined data to trigger at much faster rate
- Incompatible **readout** architecture



Figures: CERN-LHCC-2017-018 [4]

LAr New Readout at HL-LHC



Front-end (on-detector)

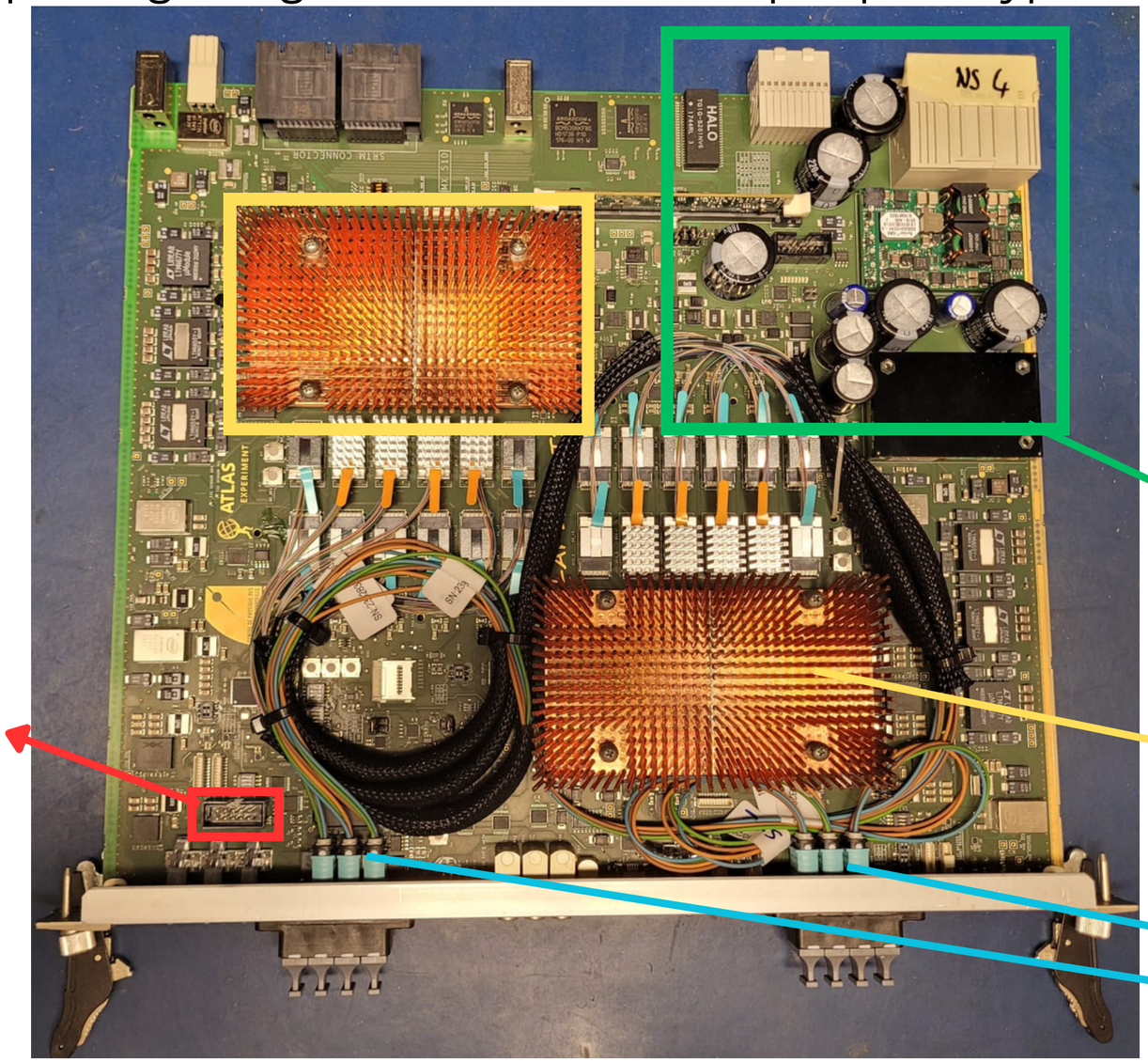
1. Triangular pulse is amplified and shaped
2. Samples and digitizes signal at 40MHz
3. Outputs from ADCs are serialized and send Off-detector via **optical links**

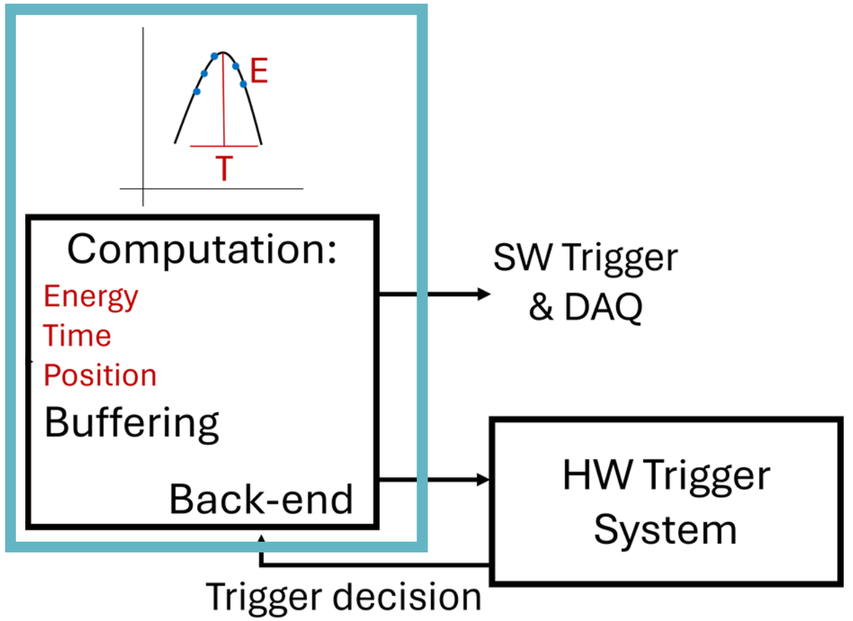
Back-end (off-detector)

1. Process ADC values to extract energy, time of each calorimeter cell
2. Information sent to trigger system at 40 MHz
3. Values are buffered awaiting trigger decision
4. Send full data stream to Data AcQuisition (DAQ)

Readout Hardware Implementation

Liquid **A**rgon **S**ignal **P**rocessor (LASP) pre-prototype board





JTAG

Power supply Capacitors

Field Programmable Gate Arrays (FPGAs) with heatsink

Optical Connections (fireflies)

Readout Hardware Implementation

Liquid **A**rgon **S**ignal **P**rocessor (LASP) pre-prototype board

Calorimeter:

182,468 cells

Front-end boards (FEB):

128 cells each

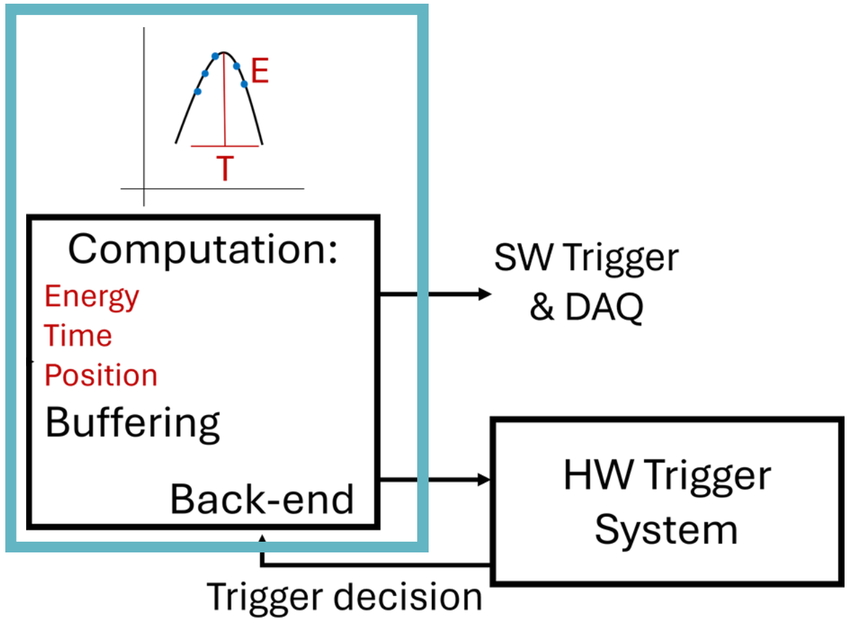
LASP FPGA:

3 FEBs

LASP Board:

2 FPGAs

Each LASP board will process 768 calorimeter cells
Input bandwidth ~1.35 Tbps!



Off-detector (Back end)

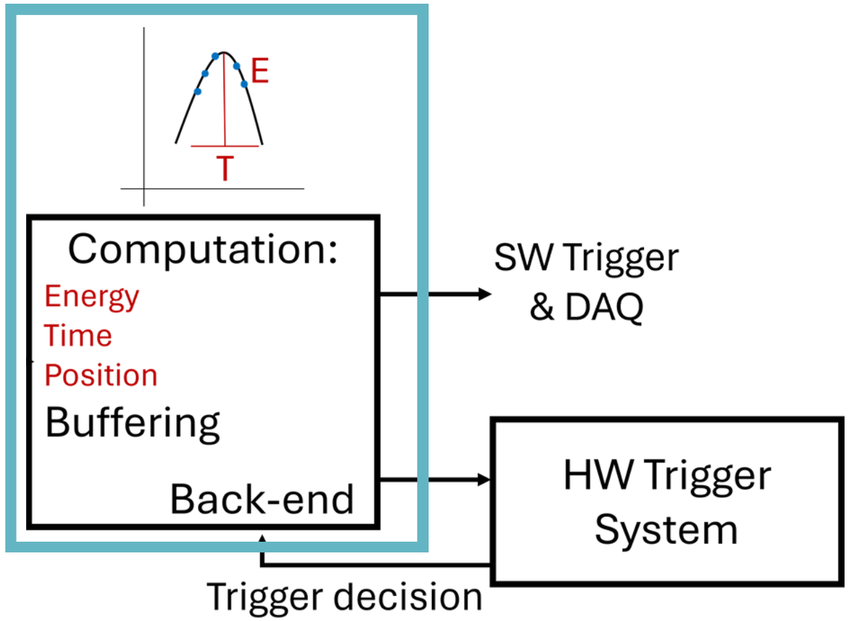
- Custom design with state of the art technology
- Prototype boards under design
- Total system will have ~300 boards

Readout Hardware Implementation

Liquid **A**rgon **S**ignal **P**rocessor (LASP) pre-prototype board

Goal

Develop infrastructure and protocols at McGill for **mass testing** of LASP production boards



Off-detector (Back end)

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Canadian LASP Testbench

Functionality

Ongoing:

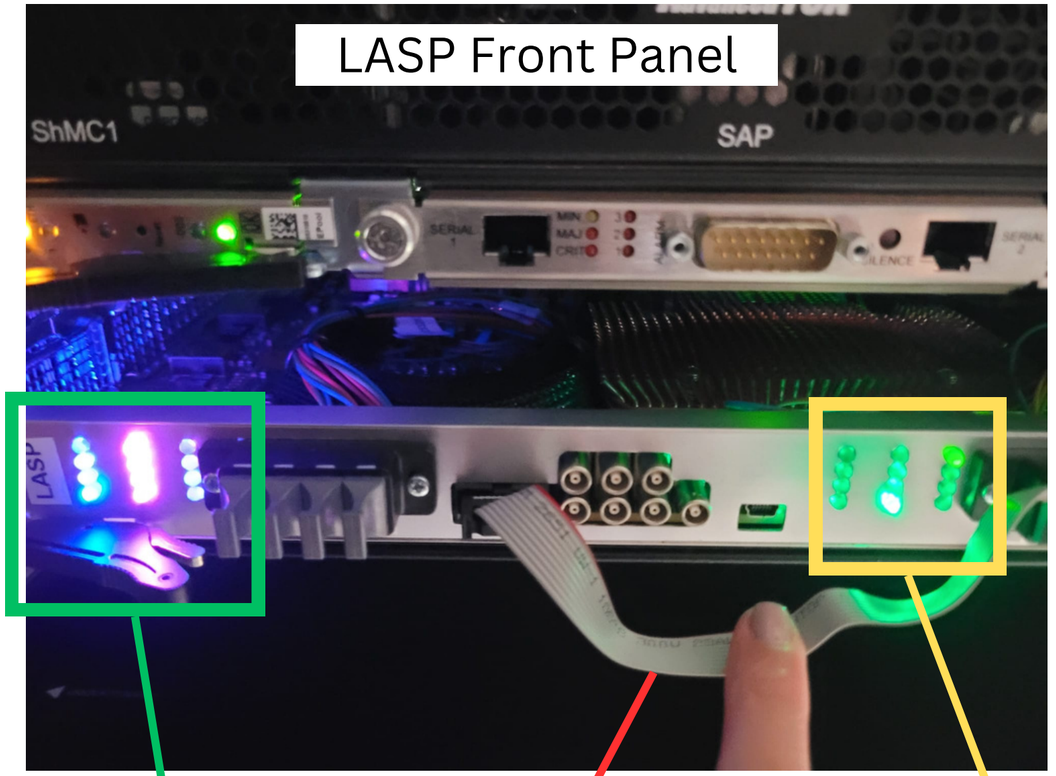
Test proper component behavior

- Power supply
- JTAG communication
- FPGAs
- Temperature Sensors

Next steps:

Early component mortality

- Stress board components



Indicate successful power supply

USB-blaster cable to JTAG connection

Indicate successful FPGA programming

Canadian LASP Testbench

Performance

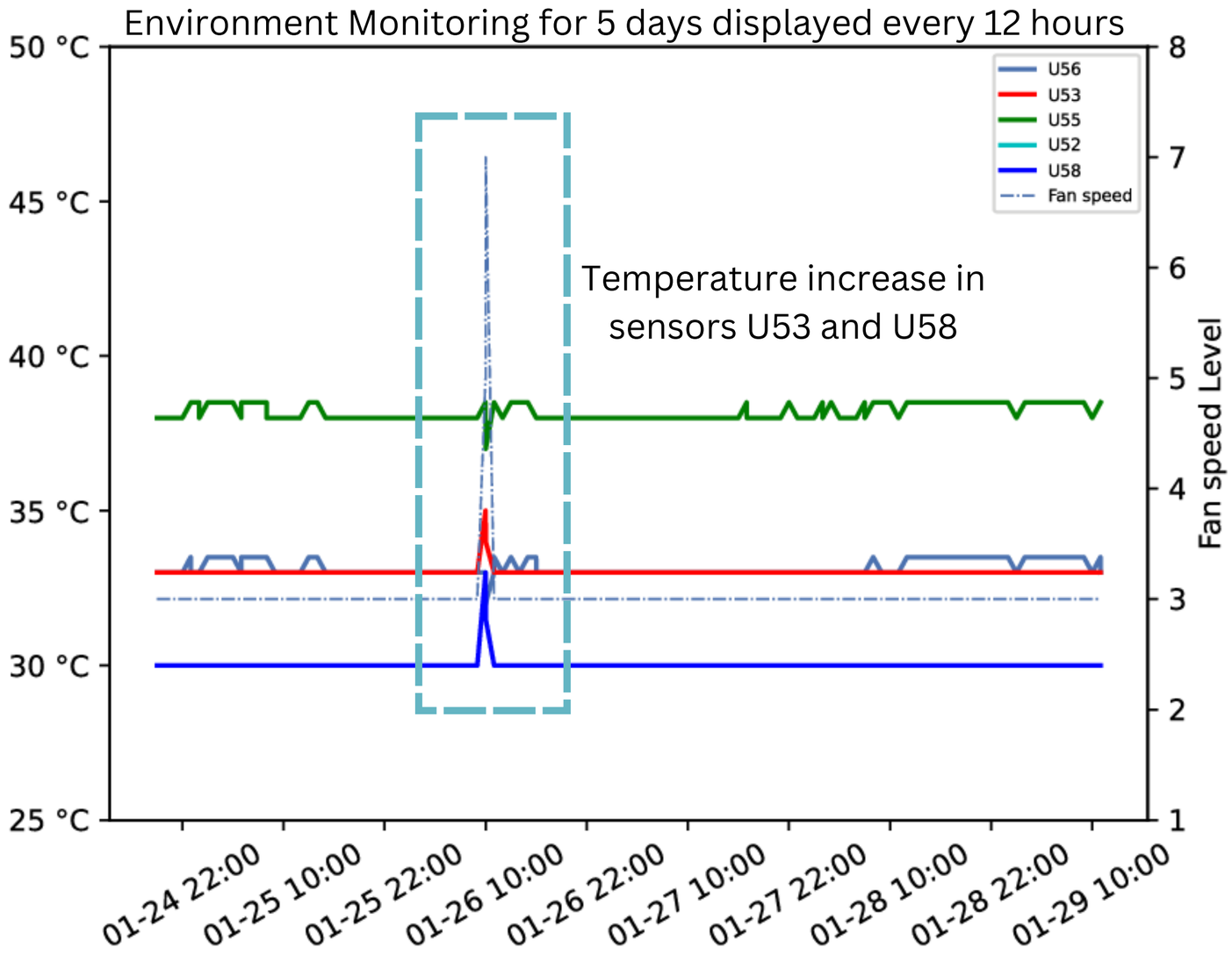
Ongoing:

Environmental Monitoring

- Temperature
- Fan speed
- Voltage
- Current

Next steps:

Board performance under maximum data input/output



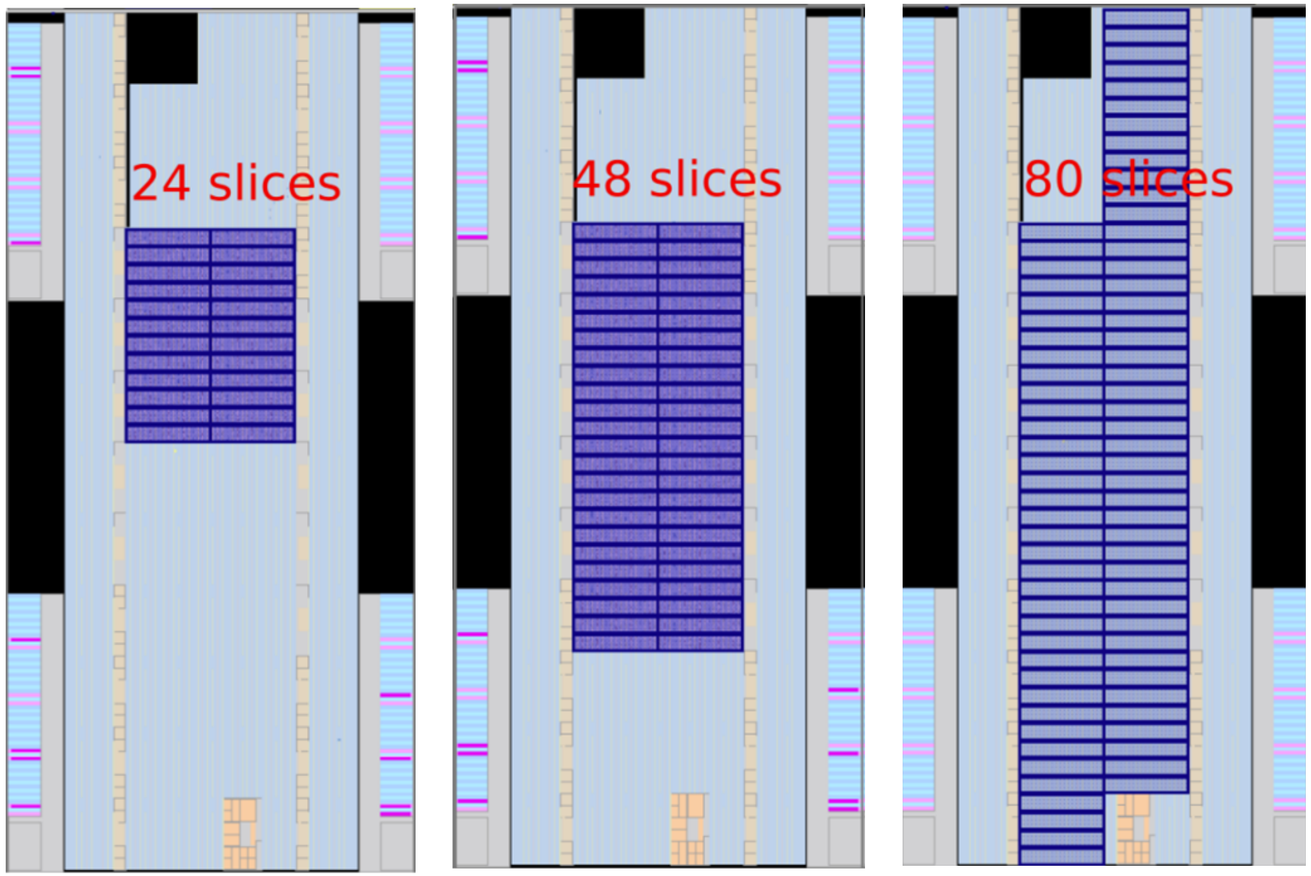
Firmware

Ongoing:

Deep testing firmware

- Find operational limits
- Evaluate power consumption of board
- Stress board components

- Initialize individual slices within FPGA fabric
- Varying resource load



Figures: Stratix 10 FPGA fabric with different number of slice compartments.
“Deep Testing FPGA Core Resource Test” by Xin Cui, McGill

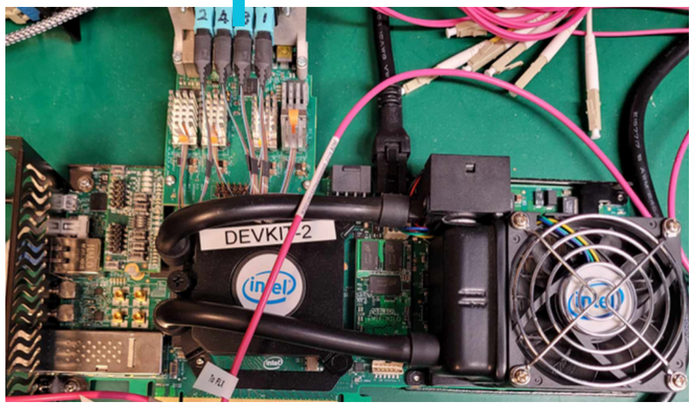
Canadian LASP Testbench

Integration

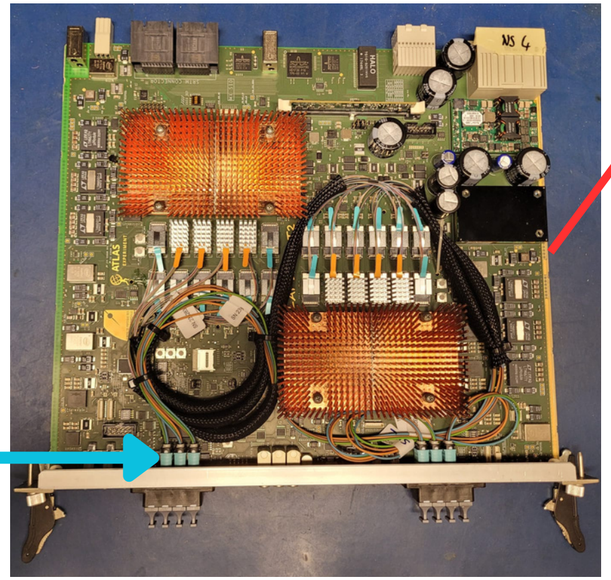
Ongoing:

- Test data stream
  - Send data to DAQ via the FrontEnd Link eXchange System (Felix)

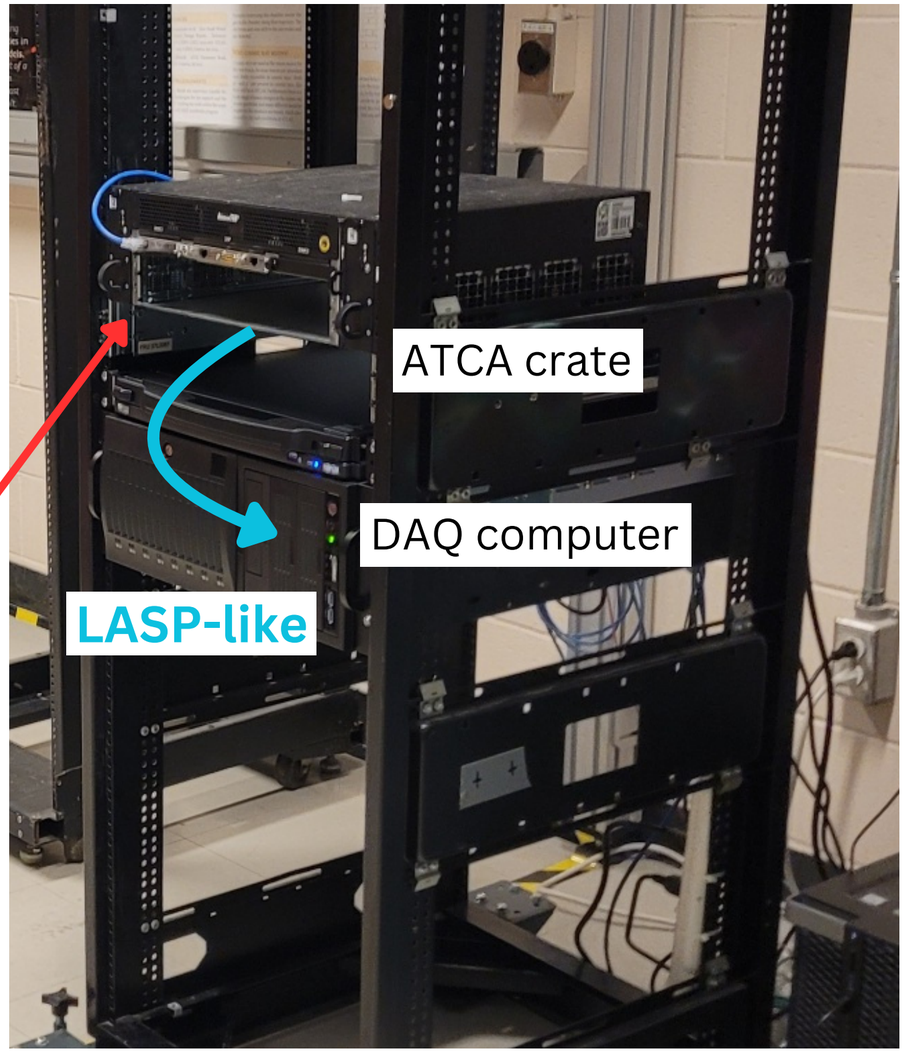
Front End Board-like



Commercially available FPGA development Kit + custom mezzanine card



LASP pre-prototype



Summary and Next Steps

- Liquid Argon Calorimeter will be upgraded for HL-LHC
  - New readout system
- New Off-detector electronic boards
  - Liquid Argon Signal Processor (LASP)
- Pre-prototype boards used for further testing
  - Hardware
  - Firmware
  - Integration

Goal: Have a fully operational testing infrastructure for the LASP production boards

Next steps:

- Determine tests and protocols
  - Early component mortality
  - Operational limits of board

Thank you!

[1] L. Evans and P. Bryant, "The CERN Large Hadron Collider: Accelerator and Experiments", JINST 3, S08001 (2008).

[2] ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider", JINST 3, S08003 (2008).

[3] J. Nielsen on behalf of the ATLAS Collaboration. "Physics Prospects for ATLAS at the HL-LHC", Journal of Physics: Conference Series, 1690, 012156 (2020).

[4] ATLAS Collaboration, "ATLAS Liquid Argon Calorimeter Phase-II Upgrade: Technical Design Report", CERN-LHCC-2017-018, Geneva, (2017).

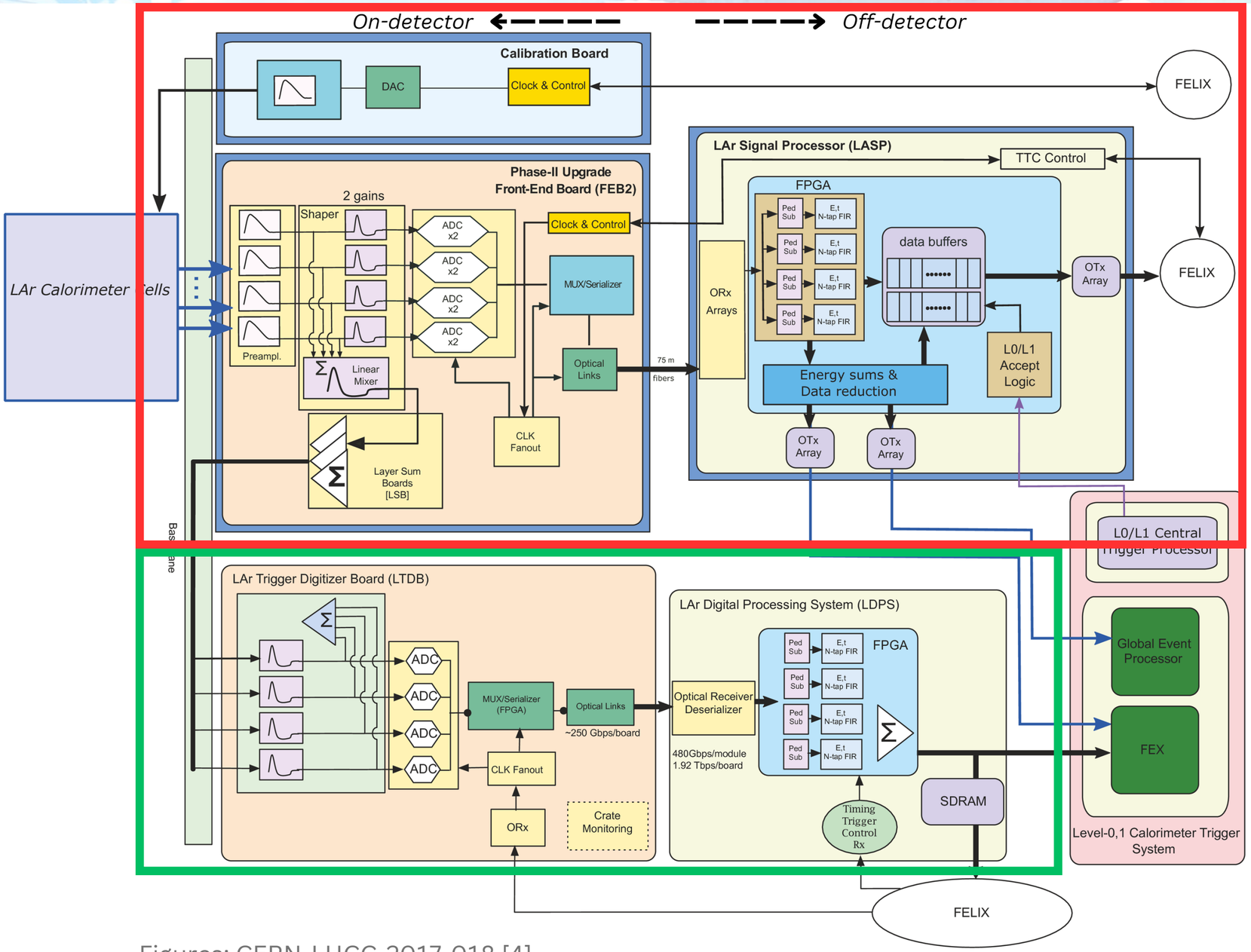
Blueprint for LAr Upgrade

Phase I Upgrades

- Digital trigger
- Comissioned

Phase II Upgrades

- **Replace** on-detector and off-detector **electronics**
- Improved radiation tolerance
- Increase frequency from 100 kHz to 40 MHz
- Increase buffering times from 2.5 us to 10 us
- Upgrade trigger rates to 1MHz

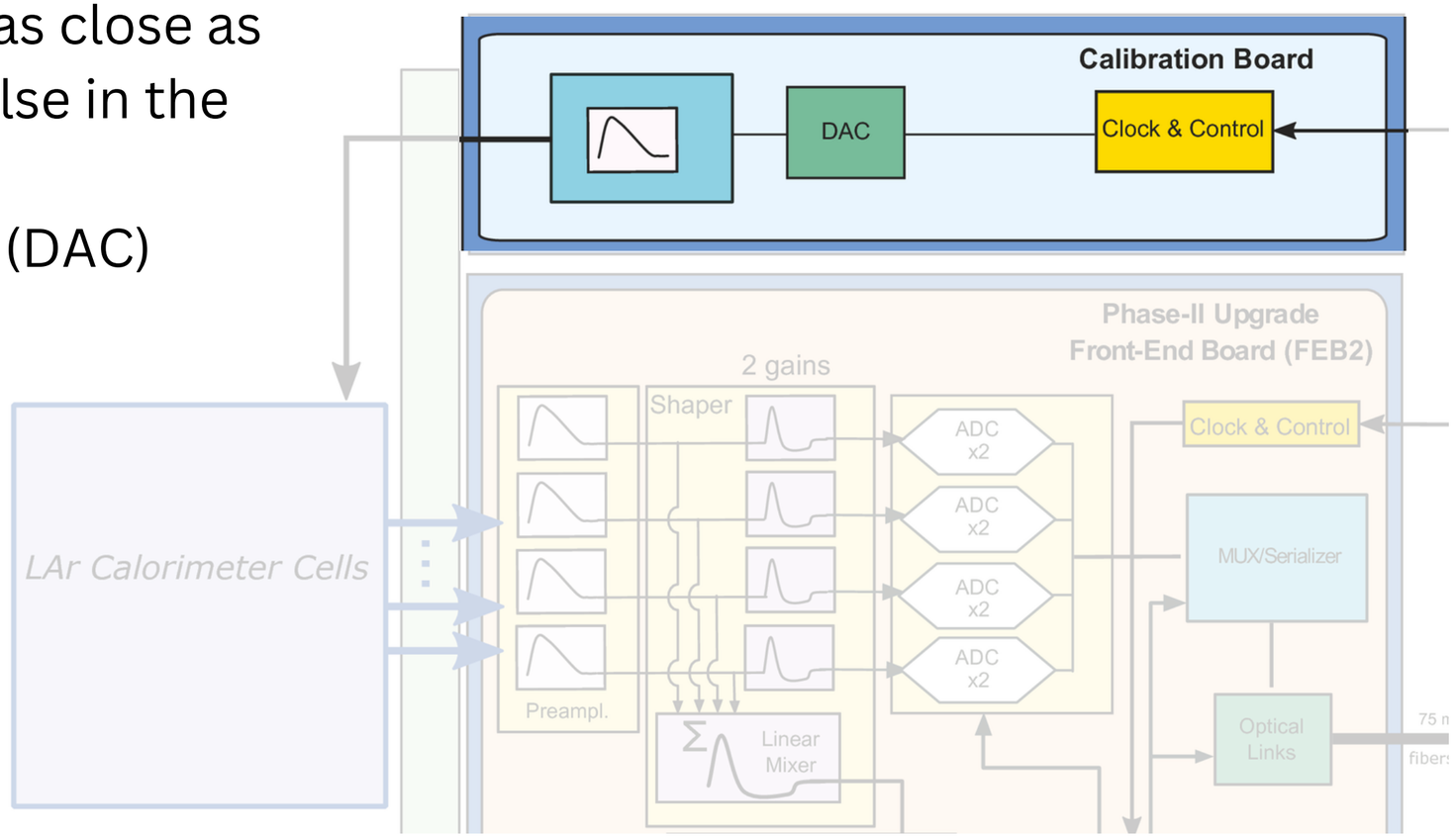


Figures: CERN-LHCC-2017-018 [4]

On-detector: Calibration Boards

Task: Inject accurate signals onto the calorimeter cells to calibrate readout

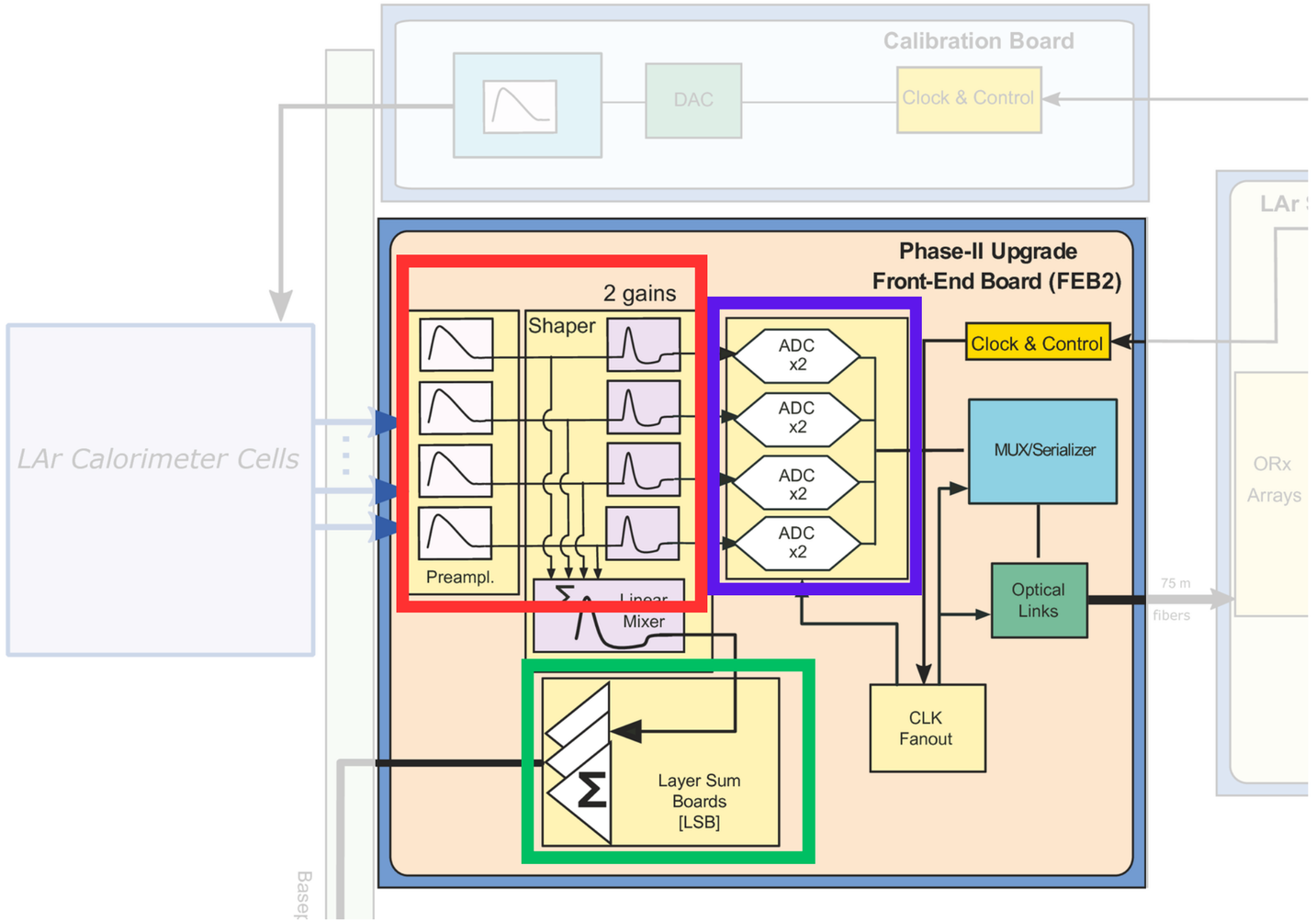
1. Produce a pulse with shape as close as possible to the ionization pulse in the detector
2. Digital-to-Analog-Converter (DAC)



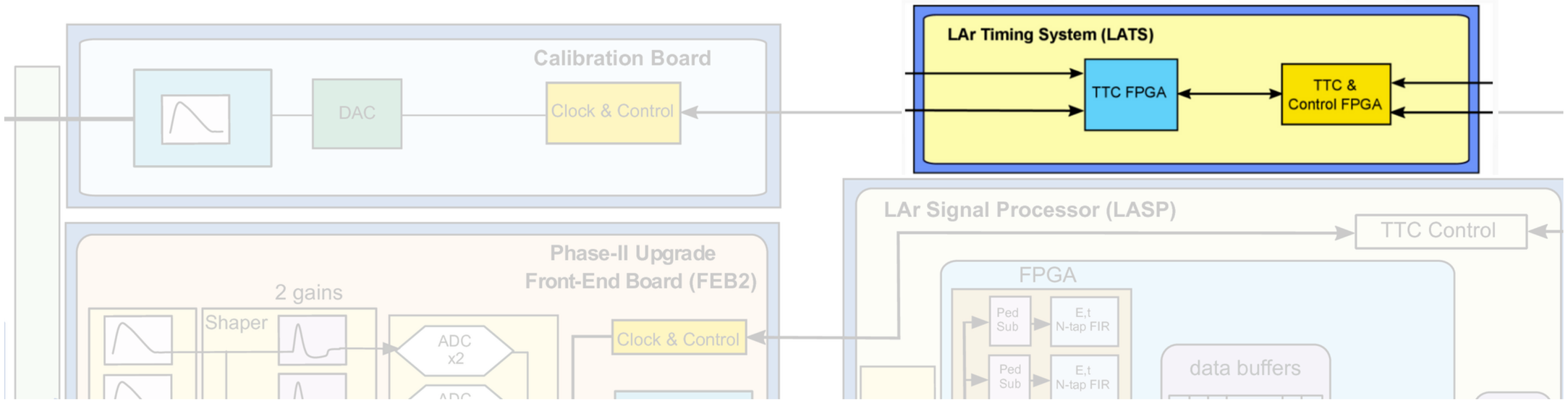
On-detector: Front End Boards (FEB2)

Task: Amplify + shape + digitize signal from calorimeter cell

1. Pre-amplifier and shaper
    a. Split signal into low gain and high gain
2. Analog-to-Digital-Converter
3. Energy sum information sent to Phase I Digital Trigger



Off-detector: LAr Timing System (LATS)



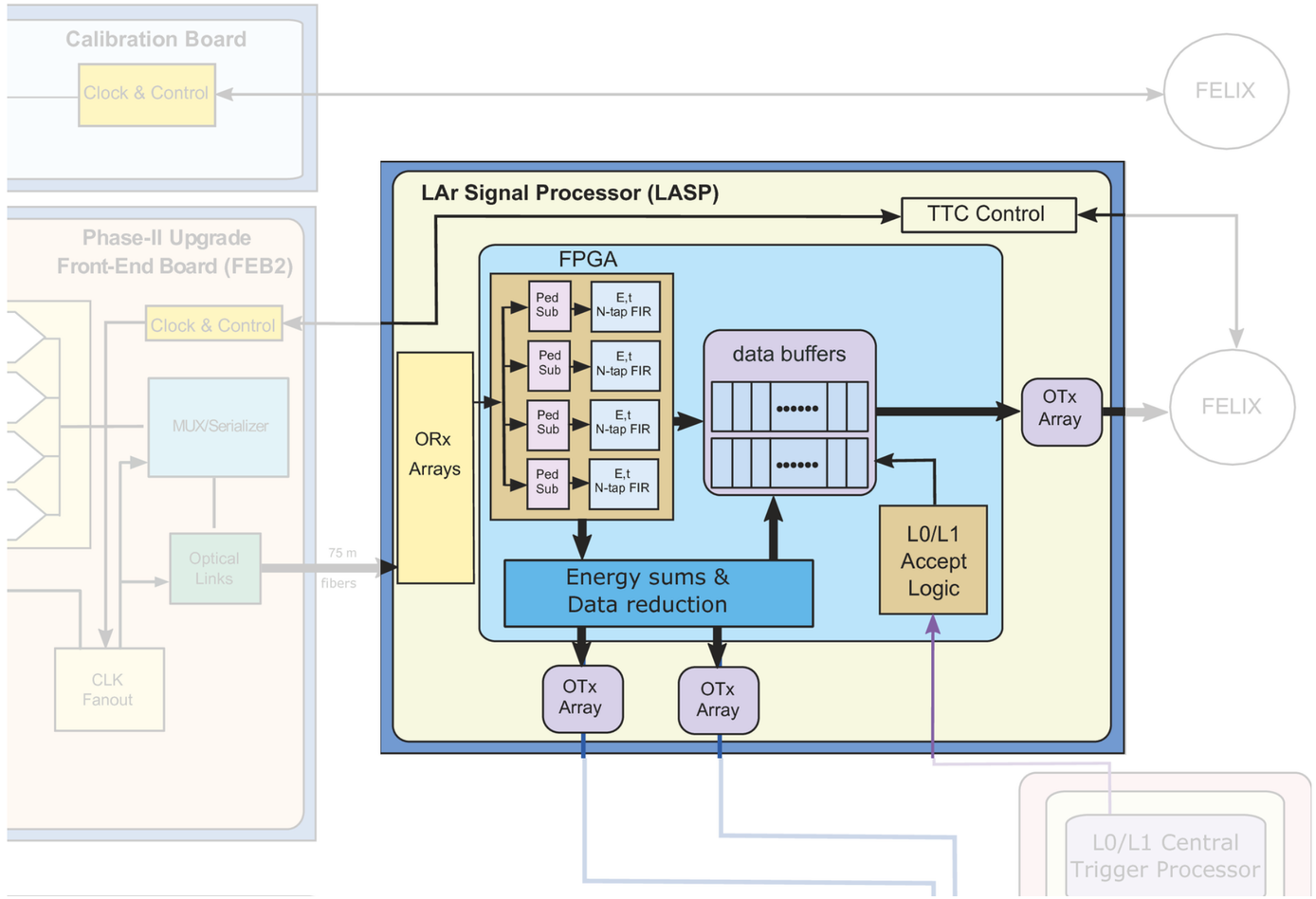
Task: Distribute TTC signal to FEB2 and Calibration Boards

TTC architecture provides distribution of synchronous **T**iming, **T**rigger and **C**ontrol signals

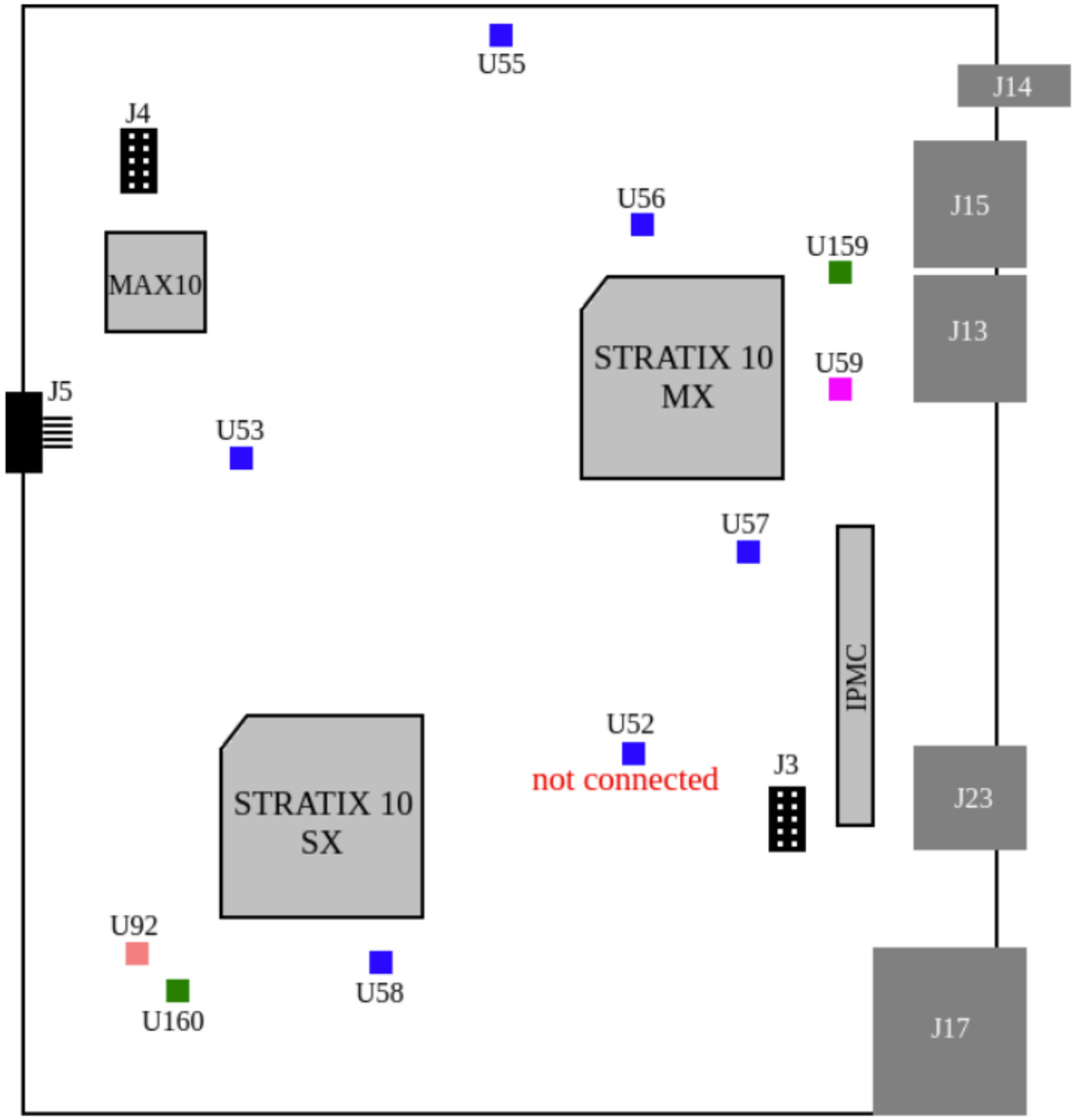
Off-detector: LAr Signal Processor (LASP)

Task: Receive front-end data from FEB2s and perform filtering

1. Receives ADCs from up to 6 FEB2 Boards
2. Applies digital filtering
3. Calculates energy, timing, and position for each signal
4. Buffer data
5. Transmits values to trigger and DAQ systems



Temperature Sensors



- **PCB sensors: TMP100**
  I2C addresses:
  - U52 : 4Fh (not connected)
  - U53 : 4Bh
  - U55 : 49h
  - U56 : 48h
  - U57 : 4Ah
  - U58 : 4Eh
- **Temperature monitor: MAX6697 for MX FPGA**
  I2C address:
  U59 : 1Ch
- **Temperature monitor: ADT7483A for SX FPGA**
  I2C address:
  U92 : 2Ah
- **Temperature monitor: LTC2990 for heatsink**
  MX FPGA heatsink:
  U159 : 4Dh

  SX FPGA heatsink:
  U160 : 4Ch

LASP Firmware and Integration Tests Status at McGill

Firmware

Program FPGAs ✓

- Test JTAG chain communication ✓
- Test Ethernet communication
- Test expected firmware behavior
- **Develop firmware needed for tests**

Integration

- Integration of multiple boards (at CERN)
- LASP to Felix computer (at McGill) ✓
- Test data stream protocols ✓
  - Mimic FEB-to-LASP
  - Mimic LASP-to-Felix

Lab Schematic